ST. ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001: 2015 Certified Institution)
ANGUCHETTYPALAYAM, PANRUTI – 607 106.

QUESTION BANK

PERIOD: JULY - NOV 2018 **BATCH**: 2017 – 2021

BRANCH: ECE **YEAR/SEM:** II/III

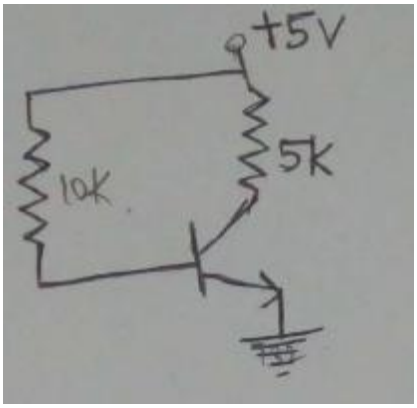
SUB CODE/NAME: EC8351 – ELECTRONIC CIRCUITS 1

UNIT I

BIASING OF DISCRETE BJT, JFET AND MOSFET

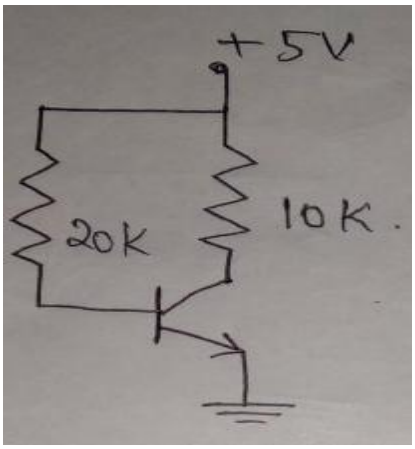
PART A

1. What is diode compensation**? [D] (April/May 2018)**
2. Sketch the fixed bias circuit of the JFET? **[D] (April/May 2018)**
3. What is the thermal runaway? **[D] (Nov/Dec 2017)**
4. List out three stability factors. **[D] (April/May 2017)**
5. Find the collector and base current of circuit given in below fig hfe = 80, Vbe(ON) = 0.7Vb [ID] **(April/May 2017)**



6. What is a Q point? **[ID] (Nov/Dec 2016)**
7. What is the impact of temperature on drain current of MOSFET? **[ID] (Nov/Dec 2016)**
8. What is an operating point? **[D] (May/June 2016, Nov/Dec 2017)**
9. Give the methods of biasing a JFET? **[D] (May/June 2016)**
10. List out the importance of selecting the proper operating point? **[ID] (April/May 2015)**
11. Define stability factor w.r.t β , Vbe , Ico **[D] (Nov/Dec 2009,Nov/Dec 2015)**
12. What is the need of a load line **[D] (Nov/Dec 2016)**
13. Define AC load line. **[D] (Nov/Dec 2016)**
14. Write the types of FET biasing. **[D] (May/June 2016)**
15. What are the parameters that affect the stability **[ID] (May/June 2014)**
16. Draw the DC load line of the circuit shown in Figure. **[ID] (April/May 2015)**

17. Find the collector and base current of circuit given in below fig hfe = 100, Vbe(ON) = 0.7V **[ID] (Nov/Dec 2014)**



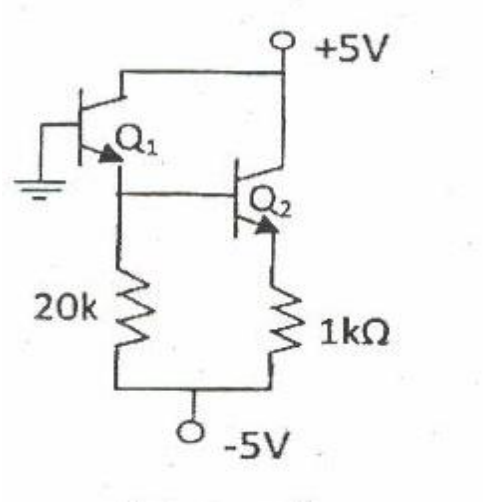
18. What are the operating regions of N-channel MOSFET and how do you identify the operating region? **[ID] (Nov/Dec 2014)**
19. Derive for the stability factor S for a fixed bias circuit. **[ID] (Nov/Dec 2010)**
20. Draw the circuit of self-bias using BJT**. [D] (May/June 2011)**
21. Write the conditions of thermal stability.**[D]**
22. Write the application of JFET. **[D]**
23. Write the general expression for stability factor. **[ID]**
24. What is the advantage of using emitter resistance in the context of biasing? **[ID]**
25. What is the impact of temperature on drain current of MOSFET? **[ID]**
26. What are the advantage and disadvantage of fixed bias. **[D]**
27. What is bias compensation using thermistor? **[D]**
28. Why is temperature compensation is required? **[ID]**
29. List out the various biasing circuits in BJT? **[D]**
30. Differentiate bias stabilization and compensation techniques. **[D]**

PART B

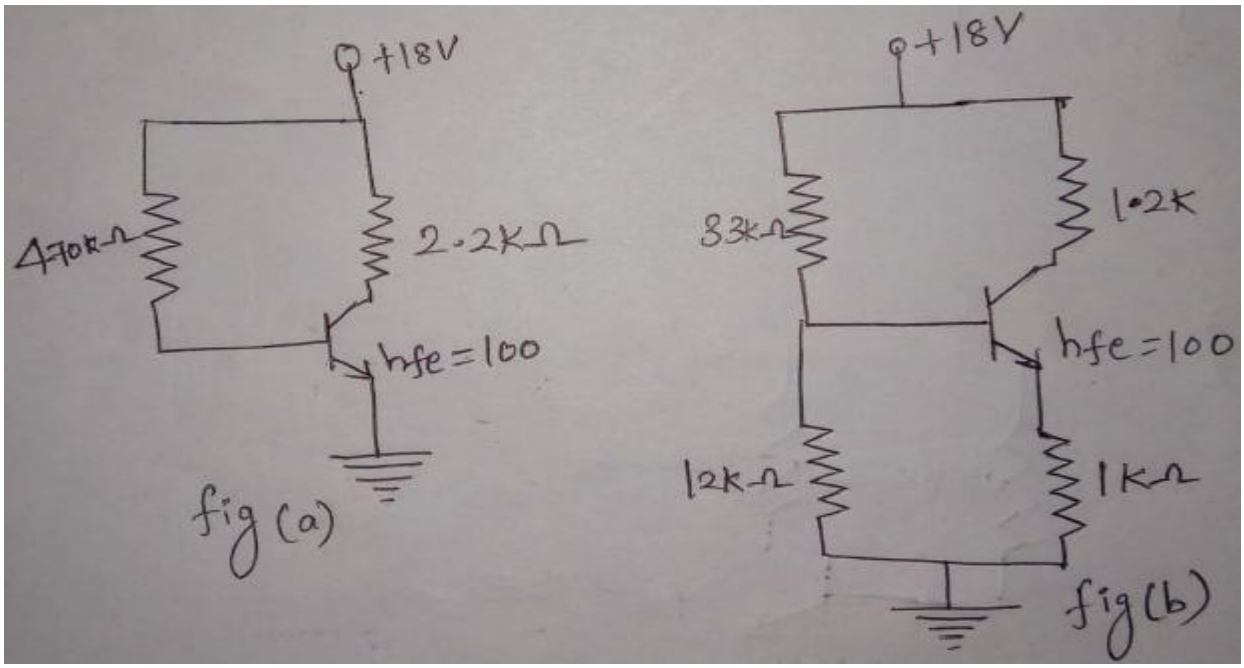
[FIRST HALF]

BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits

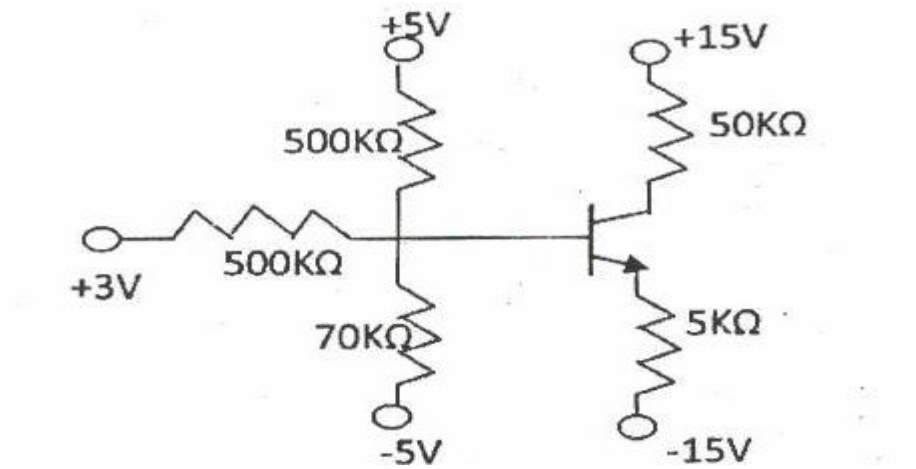
1. Briefly explain the reason for keeping the operating point of a transistor as fixed. **[ID] (7) (April/May 2017)**
2. Consider the circuit shown below with transistor parameters I_{DSS} = 12 mA, V_P = -4V, and λ = 0.008 V^{-1}. Determine the small signal voltage gain $A_v = V_o/V_i$. **[ID] (13) (Nov/Dec 2016)**
3. The parameters for each transistor in the circuit in below figure are h_{fe} = 100 and V_{BEon} = 0.7V. Determine the Q point values of base, collector and emitter currents in Q_1 and Q_2 **[ID]. (7) (April/May 2015)**



4. Determine the change in collector current produced in each bins referred to in figures (a) and (b), when the circuit temperature raised from 25°C to 105°C and I_{CBO} = 15 Na @ 25°C. **[ID] (7) (April/May 2015)**



5. Design Emitter bias for BJT with Ic = 2mA, Vcc =18V, Vce =10V and β =150. **[ID] (7) (N/D 14)**
6. The circuit in below figure let h_{fe} = 100. Find V_{TH} and R_{TH} for the base circuit. Determine I_{CQ} and $V_{CEQ.}$ Draw the DC load line. **(7) [D] (April/May 2015)**



Various biasing methods of BJT – Bias Circuit Design -

7. Compare the various methods of biasing using BJT in terms of their stability factors. **(13) [D] (May/June 2016)**
8. Explain about the voltage divider bias of BJT and derive the expression for stability factor. **(13) [D] (April/May 2018, Nov/Dec 2017, Nov/Dec 2015)**
9. Derive the stability Factors for voltage divider bias circuit and give reason why it is advantageous than fixed bias circuit. **(13) [D] (April/May 2017)**
10. Explain the fixed bias of BJT & derive the expression for stability factor **(13) [D] (May/June 2015)**
11. With a neat diagram explain the voltage divider biasing and calculate the stability factor for BJT **[D] (15) (April/May 2018, Nov/Dec 2017, Nov/Dec 2015)**

Stability factors

12. Derive the stability factor of Self bias circuit of BJT **(6) [D] (Nov/Dec 2014)**
13. Draw a self (Voltage divider bias) bias and derive the all stability factors S, S', S''. **(D)**

[SECOND HALF]

Bias compensation techniques using Diode

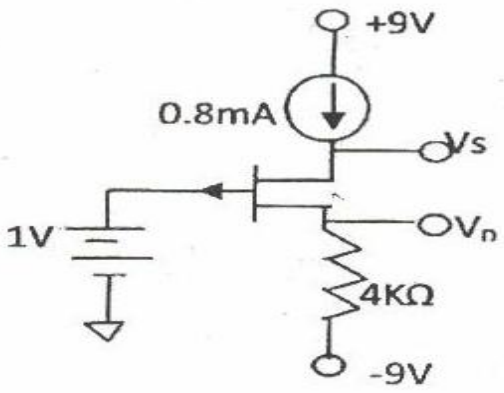
14. Draw a circuit which uses a diode to compensate for changes in I_{co}. Explain how stabilization is achieved in the circuit. **(7) [D] (April/May 2017)**
15. With neat diagram explain two bias compensation techniques and state its advantages and disadvantages. **(13) [D] (May/June 2016)**

JFET - DC Load Line and Bias Point - JFET Bias Circuit Design

16. Determine the quiescent current and voltage values in a p-channel JFET circuit**.(6) [D] (April/May 2015)**
17. What is the need for biasing, Define DC &AC load line? How JFET acts as a VVR **[ID] (Nov/Dec 2015)**

MOSFET Biasing - Biasing FET Switching Circuits.

18. With a neat diagram explain the source and drain resistance biasing of MOSFET. **(13) [D] (N/D'17)**
19. Design voltage divider bias circuit for NMOS, such that IDQ = 400 µA, VDD =14V , VDs = 2.3V, $k_n = \mu_n Cox(W / L) = 1mA / V^2$, Vt =1V .Assume a current of 1µA through R1 and R2, and Vs = 1.2 V **(13) [ID] (April/may 2015)**



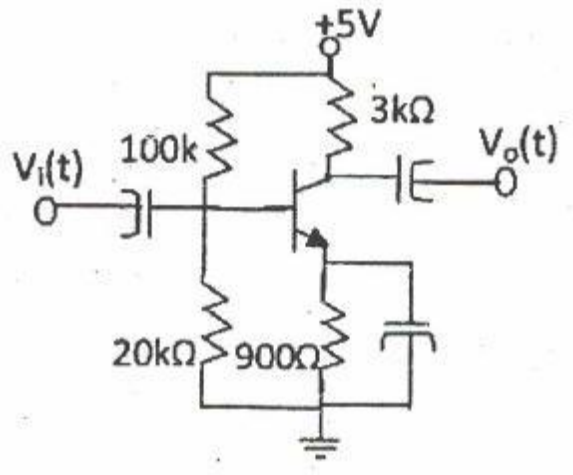
20. Analyze a BJT with a voltage divider bias circuit, and determine the change in the Q-Point with a variation in β when the circuit contains an emitter resistor. Let the biasing resistors be R_{B1} = 56KΩ, R_{B2} = 12.2KΩ, R_c = 2KΩ, R_E = 0.4KΩ, V_{cc} = 10V, V_{BE}(on) = 0.7V, and β = 100. **(15) [D] (Nov/Dec 2016)**

UNIT- II

BJT AMPLIFIERS

PART A

1. Why CE configuration is preferred for Amplification? **[ID] (Apr/May 2018)**
2. What is bypass and coupling capacitor? **[D] (Nov/Dec 2017)**
3. List the need for bootstrapping in amplifier? **[ID] (Nov/Dec 2017)**
4. Define millers theorem **[D] (May/June 2010, Nov/Dec2015, April/May 2017)**
5. Draw the small signal ac equivalent circuit of the BJT. **[D] (Nov/Dec 2016, April/May 2017**)
6. What is an ac load line. **[D] (Nov/Dec 2016)**
7. What is the need of load line**. [ID] (May/June 2016)**
8. Draw a cascade amplifier and its ac equivalent circuit. **[D] (May/June 2016, April/May 18)**
9. Define CMRR of BJT differential amplifier. How it improved? **[ID] (Apr/May 2015, Nov/Dec 2016)**
10. A small signal source $V_i(t) = 20\cos 20t + 30\sin 10^6 t$ is applied to a transistor to a transistor amplifier as shown in below fig. The transistor has h_{fe} = 150, $r_0 = \infty$ and $R\pi$ = 3KΩ. Determine $V_0(t)$. **[ID] (Apr/May 2015)**



11. Draw the hybrid model of CE amplifier **[ID] (Nov/Dec 2009, Nov/Dec2016)**
12. State the various methods of improving CMRR. **[ID] (Nov/Dec 2014)**
13. List out the advantages of h parameters **[D] (Nov/Dec 2014)**
14. Find CMRR of differential amplifier with differential gain of 300 and common mode gain of 0.2. **[ID] (Nov/Dec 2014)**
15. Write the characteristics of CE amplifier **[D] (May/June 2014)**
16. Draw the hybrid model of CC amplifier. **[D]**
17. Draw the circuit diagram of Darlington type amplifier **[D] (May/June 2013)**
18. Write the characteristics of CC amplifier **[D] (Nov/Dec 2013)**
19. How are amplifiers classified according to the transistor configuration **[ID] (Nov/Dec 2015)**
20. What is Darlington Connection **[D] (May/June 2014)**
21. What are the Coupling schemes used in multistage amplifiers **[D] (May/June 2010)**
22. Draw the circuit diagram of Darlington type amplifier **[D] (May/June 2013)**
23. Draw a Darlington amplifier with Bootstrap Management **[ID] (Nov/Dec 2010)**
24. Write the characteristics of CC amplifier **[D] (Nov/Dec 2013)**
25. What is the advantage of Darlington amplifier **[D] (Nov/Dec 2013)**
26. What is the main application of CB configuration of transistor **[ID]**
27. What are the limitations of h-parameters **[D]**
28. Draw the hybrid model of CC amplifier **[D]**
29. What is bootstrapping. **[D]**
30. Why constant current source biasing is preferred for differential amplifier

PART B

[FIRST HALF]

Single stage and Multi-stage amplifier

1. Compare and contrast of single stage and Multistage amplifier. **[D] (15) (April/may 2018)**

Analysis of CE, CC and CB amplifiers using Hybrid π equivalent circuits

2. Derive the expressions for the voltage gain, current gain, input and output impedance of emitter follower amplifier. **(13) [D] (April/May 2018)**
3. Draw the a.c equivalent circuit of a CE amplifier with voltage divider bias and derive the expression for current gain, voltage gain, input impedance, output admittance and overall current gain. **(13) [D] (April/May 2017)**
4. Explain about CB amplifier and derive the expression for gain, Ri, Ro. **(13) [D] (Nov/Dec 2016)**
5. Explain about CE amplifier with emitter resistor and an emitter bypass capacitor are incorporated in the design? Explain with necessary equations. **(13) [D] (Nov/Dec 2014, (May/June 2016)**

6. Compare CB, CE and CC amplifiers and state their applications **(7) [D] (May/June 2012)**
7. Calculate the small signal voltage gain of an emitter follower circuit. Given $\beta=100, V_{BE}=0.7V, V_A=80V, I_{CQ}=0.793mA, V_{CE}Q=3.4V$. **(7) [ID]** (**May/June 2016)**
8. What are the changes in the a.c characteristics of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design? Explain with necessary equations. **[ID]** (**May/June 2016)**

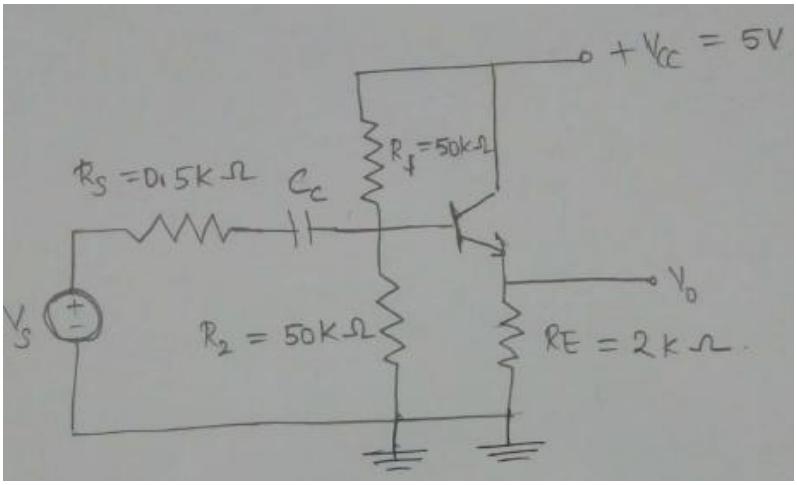
Darlington Amplifier - Bootstrap technique

9. Draw and explain the operation of a Darlington amplifier. **(7) [D]** (**May/June 2016)**
10. Explain the boot strapped Darlington emitter follower with circuit diagram **(13) [ID] (N/D 14)**.
11. With neat diagrams, explain the operation and advantages of Darlington pair circuit. Also analyze its small-signal voltage gain and input impedance**. (13) [ID] (Nov/Dec 2016)**

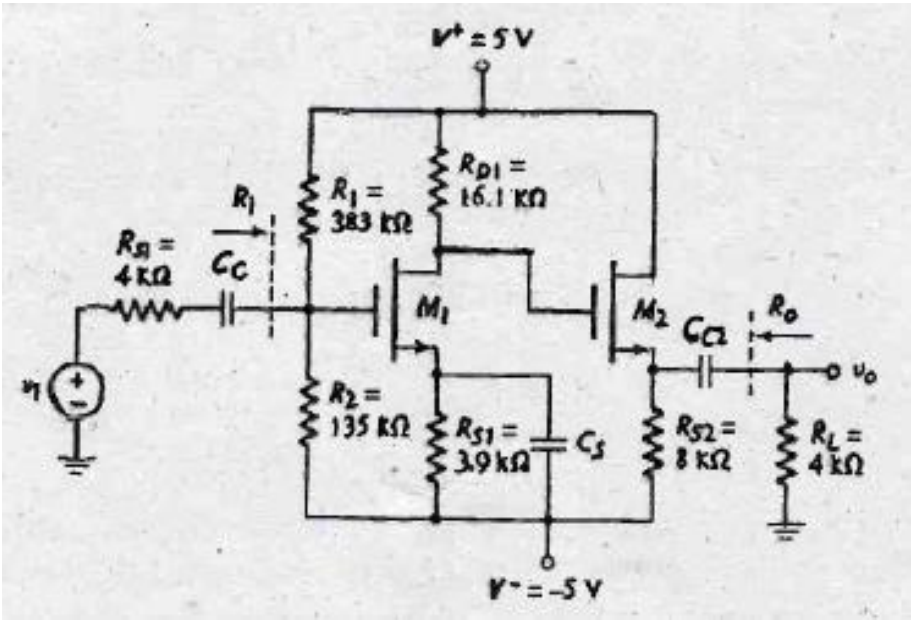
[SECOND HALF]

Cascade and Cascode configurations

12. Write short notes on multistage amplifiers. Draw a two stage RC coupled amplifier and explain. Also compare Cascade and Cascode amplifier. **(13) [D] (April/May 2018)**
13. (i) Explain the operation of Cascode amplifier and derive gain, input impedance and output impedance **(13) [D] (Nov/Dec 2014)**
14. Consider the circuit shown in fig with the parameters are h_{fe} = 120, $V_0 = \infty$. Determine the current gain, voltage gain, input impedance and output impedance. Find the maximum undistorted output voltage swing. **(13) [ID] (April/May 2015)**
15. Compare and contrast on the design of bandwidth of the single stage and multi stage amplifiers. **(15) [D] (April/May 2018)**
16. What is Cascade Amplifier? Explain with necessary equations and explain how to determine its bandwidth. **(15) [D] (Nov/Dec 2017)**
17. Calculate the input and output resistance of the emitter- follower circuit shown in below Fig. Assume R3 = 0.5 k, $r\pi$ = 3.28 KΩ, β =100 and Ro =100 KΩ. **(15) [ID] (April/May 2017)**



18. Determine the small signal voltage gain of a multistage cascade circuit shown in the figure below. The transistor parameters are $K\alpha 1 = 0.5$ mA/V^2, $K\alpha 2 = 0.2$ mA/V^2, $V_{TN1} = V_{TN2} = 1.2$ V and $\lambda_1 = \lambda_2 = 0$. The quiescent drain currents are $I_{D1} = 0.2$ mA and $I_{D2} = 0.5$ mA. **(13) [D] (Nov/Dec 2016)**



Differential amplifier

19. Summarize the working principle of CMOS differential amplifier with the neat diagram. Also determine its CMRR. **(15) [ID] (April/May 2018, Nov/Dec 2017)**
20. Explain in detail the transfer characteristics of differential amplifier. Explain the method used to improve CMRR. **(16) [ID] (Nov/Dec 2015)**

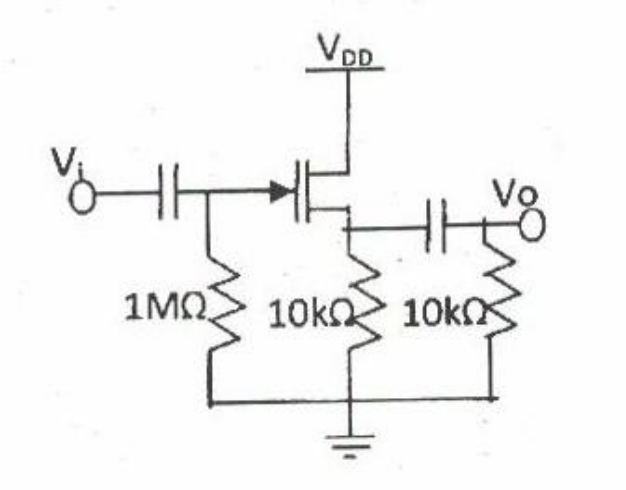
UNIT-III

SINGLE STAGE FET, MOSFET AMPLIFIERS

PART A

1. What is IDSS in a JFET? **[D] (April/May 2018)**
2. Why MOSFETs are used? **[ID] (April/May 2018)**
3. What is BiMOS? **[ID]** (**May/June 2016) (Nov/Dec 2017)**
4. A self biased P -channel JFET has a pinch off voltage of 5V and $I_{DSS} = 12$ mA. The supply voltage is 12 V. Determine the value of resistors R_D and $R_{S,\ So}$ that $I_{D\ =} 5$ mA and $V_{DS\ =} 6$ V. **[ID] (Nov/Dec 2017)**
5. What are the features of BiMOS cascode amplifier. **[ID] (April/May 2017, N/D 2014)**
6. What is the use of source bypass capacitor in CS amplifier. **[ID] (April/May 2017)**
7. What is the impact of including a source resistor in the FET amplifier **[ID] (Nov/Dec 2016)**
8. Why multistage amplifiers is required? **[ID] (Nov/Dec 2016)**
9. What is body effect in MOSFET **[ID] (May/June 2016)**
10. Give the general condition under which common source amplifier would be used. **[ID] (M/J 16).**

11. Compare between JFET and MOSFET **[D] (Apr/May 2015)**
12. Determine the output impedance of a JFET amplifier shown in fig. Let $g_m = 2$ mA/V and $\lambda = 0$ **[ID] (Apr/May 2015)**



13. Draw the small signal equivalent model of JFET. **[D] (Nov/Dec 2014)**
14. Write the characteristics of common source MOSFET amplifier. **[ID]**
15. Write the characteristics of MOSFET source follower amplifier. **[ID]**
16. Draw the equivalent circuit of common source MOSFET amplifier. **[D]**
17. Draw the equivalent circuit of common gate MOSFET amplifier. **[D]**
18. What are the three types of MOSFET amplifiers **[D]**
19. Draw the BICMOS Darlington pair configuration **[D]**
20. List the three basic JFET basic configurations? **[D]**
21. Write the three FET parameters. **[D]**
22. Define transconductance. **[D]**
23. Define drain resistance. **[D]**
24. Define amplification factor. **[D]**
25. What are the three types of MOSFET amplifiers **[D]**
26. Draw the equivalent circuit of CS FET. **[D]**
27. What do you mean by non unilateral amplifiers **[ID]**
28. What do you mean by unilateral amplifiers **[ID]**
29. What are the features of bipolar cascode configuration **[D]**
30. Give the expression for Av and Ai for NMOS common gate amplifier **[ID]**

PART B

[FIRST HALF]

Small Signal Hybrid π equivalent circuit of FET and MOSFET

1. Describe the small signal equivalent circuit of the MOSFET and determine the values of small signal parameters**. (13) [D] (April/May 2018)**

2. Enumerate on voltage swing Limitations, general conditions under which a source follower amplifier would be used. **(OR)** With a neat diagram explain the source follower amplifier using MOSFET and derive the necessary equations to calculate the voltage gain input and output resistance. **(13) (April/May 2018) [D] (Nov/Dec 2014)**
3. Draw a small signal low frequency model for an FET and Explain. **[D] (6)**
4. Draw the characteristics of JFET and mark its region of operation. **[D] [4]**

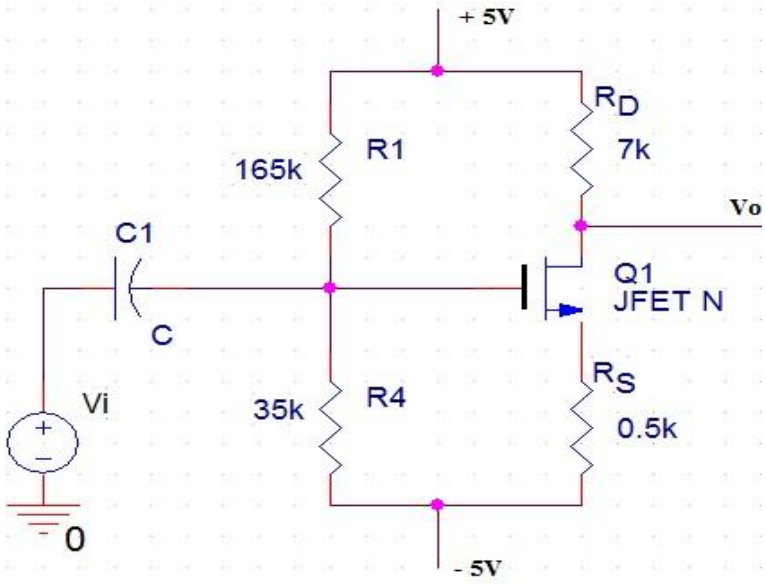
Analysis of CS, CD and CG amplifiers using Hybrid π equivalent circuits

5. With a neat diagram small signal analysis of common source amplifier with a source resistance for MOSFET. **(13) [D] (Nov/Dec 2017)**
6. Explain about MOSFET CG amplifier and derive the expression for gain, input impedance and output impedance**. (13) [D] (Nov/Dec 2015. April/May 2017)**
7. Draw the circuit of a basic common source amplifier with voltage divider bias and derive the expression for voltage gain, input impedance and output impedance using small-signal model**. (7) (Nov/Dec 2014, Nov/Dec 2016)**
8. Explain about MOSFET CS amplifier and derive the expression for gain, input impedance and output impedance. **(13)**
9. Explain in detail about voltage swing limitations. **(6)**
10. Compare in detail about CG, CD, CG amplifier. **(7)**
11. Determine the voltage gain of the circuit assuming the following parameters V_{Do} = 3.3 V, R_D = 4 KΩ, R_{G1} = 10 KΩ, R_{G1} = 60 KΩ, R_{G1} = 10 KΩ, R_{Si} = 4 KΩ. The transistor parameters are: V_{TN} = 0.4 V, K_a = 0.5 mA/V^2, and λ = 0.02 V^{-1}. **(7) [D] (Nov/Dec 2016)**
12. Enumerate in detail and derive expression for voltage gain of CS and CD amplifier under small signal low frequency condition. **(13) [D] (Nov/Dec 2015)**

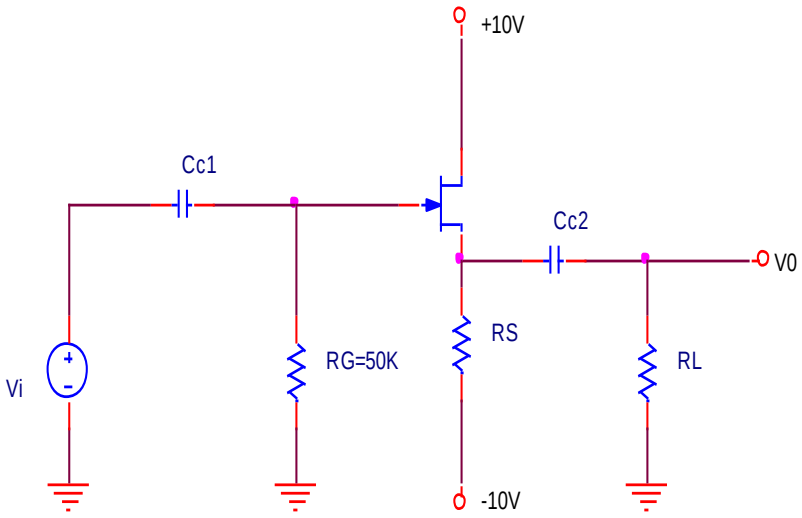
[SECOND HALF]

Basic FET differential pair

13. Derive gain, input and output impedance of common source JFET amplifier with neat diagram and equivalent circuit. (13) [D] (April/May 2017, Nov/Dec 2014)
14. Draw a discrete JFET CG amplifier and derive the expression for gain, input impedance and output Impedance small signal equivalent circuit. **(6) [D] (Apr/May 2015)**
15. Determine the current gain of JFET source follower amplifier**. (6) [D] (Apr/May 2015)**
16. Derive a small signal low frequency model for an FET and explain. **(13) [D] (Nov/Dec 2009)**
17. Determine the small signal voltage gain of a common source circuit containing a source resistor. The transistor parameters are V_{TN}=0.8V, Kn=1mA/V^2 and λ=0 **(15) [D] (May/June 2016)**

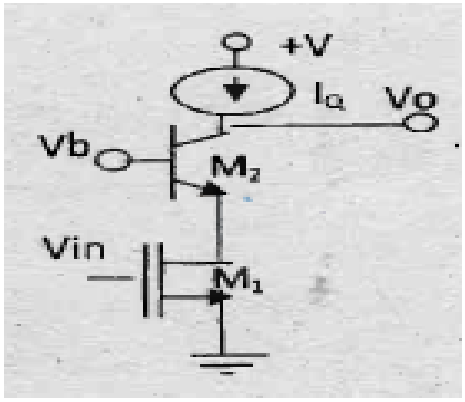


18. Design a JFET source follower circuit with a specified small voltage gain given I_{DSS}=12mA,Vp=-4V,λ=0.01V^{-1}. Determine Rs and I_{DQ} such that the small voltage gain is at least A_v=0.90 **(15) [D] (May/June 2016)**



BiCMOS circuits.

19. Explain the operation of BIMOS cascode amplifier with a neat diagram**. [D] (Nov/Dec 2015)**
20. Derive the voltage gain of BiCMOS cascade amplifier shown in fig. **(13) [D] (Apr/May 2015)**



UNIT IV

FREQUENCY RESPONSE OF AMPLIFIERS

PART A

1. Define 3 db frequency? **[ID] (April/May 2018)**
2. What is beta frequency? **[D] (April/May 2018)**
3. What is Miller effect? **[D] (Nov/Dec 2017)**
4. What is Unity gain of amplifier? **[ID] (Nov/Dec 2017)**
5. Define rise time**.** Give relation between rise time and bandwidth **[ID] (April/May 2017)**
6. Draw the hybrid π equivalent circuit of BJT **[D] (Nov/Dec 2015, Nov/Dec 16, Apr/May 17)**
7. What is the reason for reduction in gain at lower and higher frequencies in case of amplifiers. **[ID] (Nov/Dec 2016)**
8. Determine the unity gain bandwidth of a FET with parameters, Cgd=10fF, Cgs=50fF and g_m = 1.2 mA/V. **[ID] (Nov/Dec 2016)**
9. A bipolar transistor has parameter βo= 150, Cπ=2pF, Cμ=0.3pF and is biased at I_{CQ} = 0.5 mA. Determine the cut off frequency. **[ID] (April/May 2016)**
10. Find the unity gain bandwidth of a MOSFET whose, C_{ds} = 1 pf, Cgd =10 pF, Cgs= 8pF and g_m = 6 mA/V. **[ID] (April/May 2015)**
11. The ac schematic of an NMOS common source stage is shown in the fig where part of the biasing circuits has been omitted for simplicity. For the N – channel MOSFET M_1, the transconductance, g_m = 1 mA/V, and body effect and channel length modulation effect are to be neglected. Find the lower cutoff frequency. **[ID] (April/May 2015**)
12. What is the effect of Millers capacitance on the frequency response of an amplifier **[D] (Nov/Dec 2014)**
13. Relate gain and bandwidth of single and multi-stage amplifier. **[ID] (Nov/Dec 2014)**
14. The rise time of BJT is 40ns, what is the bandwidth by using this BJT **[D] (May/June 2012)**
15. Give the equation of overall upper cutoff frequencies and lower cutoff frequencies of multistage amplifier **[ID] (May/June /2008)**
16. Draw the high frequency model for FET **[D] (May/June 2012)**
17. What is a miller capacitance of a transistor? **[D]**
18. Define the frequencies f_T & f_β **[ID]**
19. Draw the frequency response of amplifiers. **[D]**
20. In an amplifier the maximum voltage gain is 2000, occurs at 2KHz. It falls to 1414 at 10Hz and 50Hz.Find i) B.W ii) Lower and upper cut off frequency. **[D]**
21. A three stage amplifier has a first stage voltage gain of 100, second stage voltage gain is 200 & third stage gain of 400.Find the total voltage gain in db. **[ID]**
22. What is the bandwidth of an amplifier. **[D]**
23. What is the relationship between bandwidth and rise time. **[ID]**
24. Define sag in an amplifier. **[ID]**

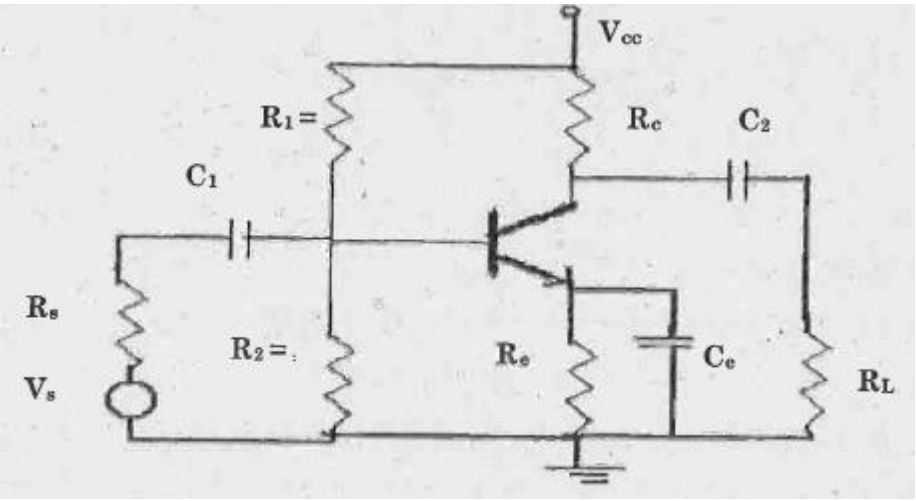
25. What is meant by gain bandwidth product.**[ID]**
26. Discuss the effect of bypass capacitor on frequency response of amplifier. **[ID]**
27. Why is not possible to use the h parameters at high frequencies. **[D]**
28. Give the expression for gain bandwidth product for voltage and current. **[D]**
29. What do you mean by unity gain frequency? **[D]**
30. List the various gate capacitances in MOSFET. **[D]**

PART B

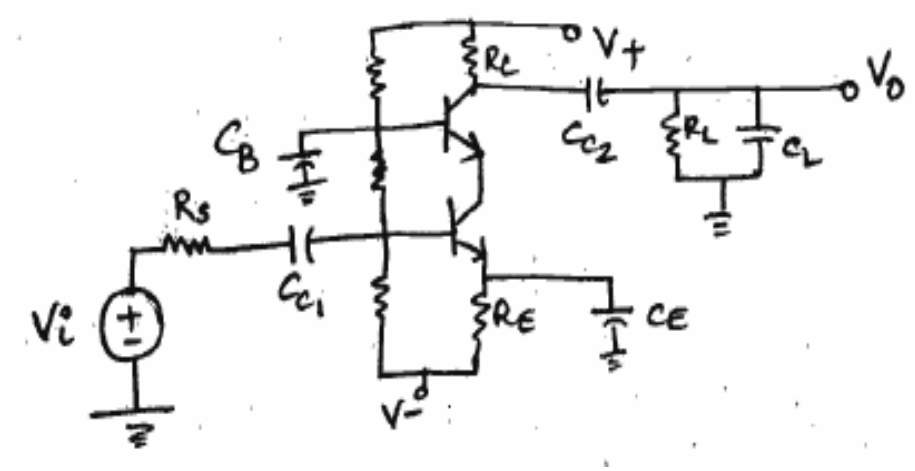
[FIRST HALF]

Frequency response of transistor amplifiers with circuit capacitors

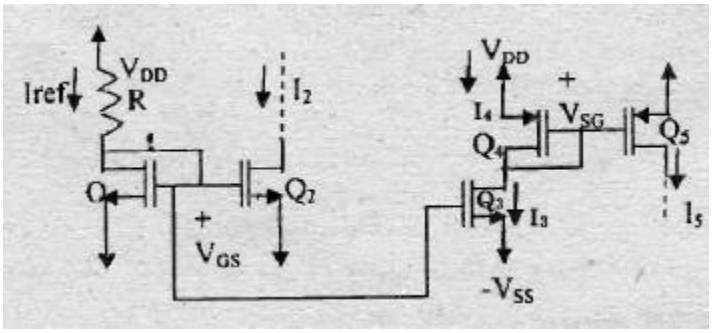
1. With neat sketch, explain hybrid π CE transistor model. Derive the expression for various components in terms of h parameters **(13) [D] (April/May 2018, Nov/Dec 2015)**
2. Explain the high frequency response of common emitter amplifier and derive the necessary equation to calculate the upper 3 DB frequency. **(13) [ID] (Nov/Dec 2017)**
3. Determine the low frequency response of the amplifier circuit shown in Fig.Given data's R_S = 680 Ω; Rl = 68 K Ω; R2 = 22K Ω; Re = 1K ; Vcc, =10 V , C1=C2=0.11μF;C_E=10μF. R_C=2.2 K Ω; R_L =10 K Ω ;β =100, hie = rπ =1.1 k **(13) [ID] (April/May 2017)**



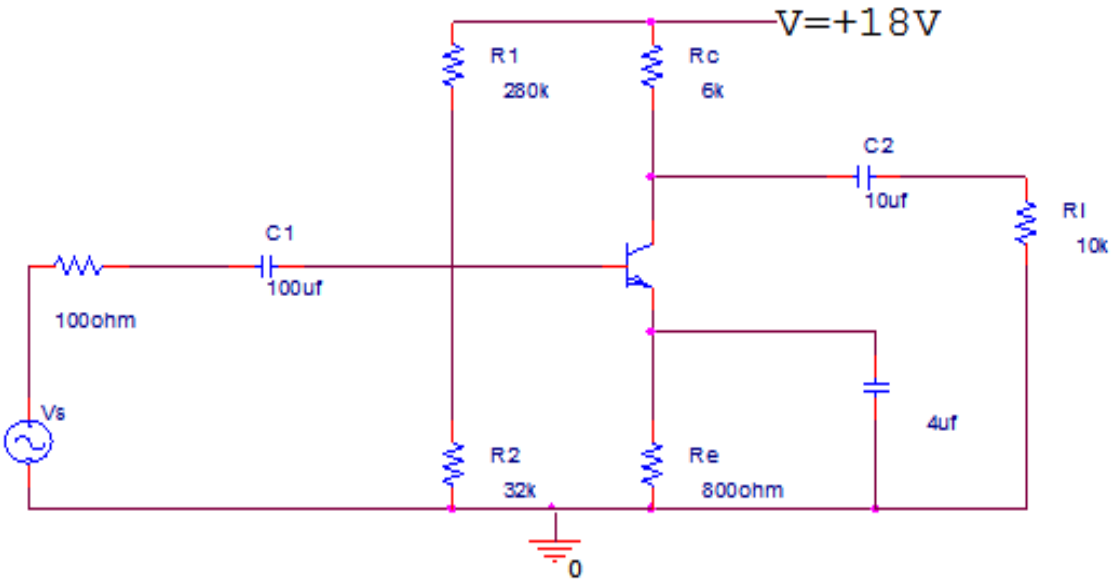
4. Determine the 3 dB frequencies and mid band gain of a cascade circuit.for the figure the parameters are V^+=10V, V=-10V, R_s=0.1kΩ, R_1=42.5kΩ, R_2=20.5kΩ R_3=28.3kΩ, R_E=5.4kΩ, R_C=5kΩ, R_L=10kΩ, C_L=0.the transistor parameters are β =150, $V_{BE(ON)}$=0.7 V, V_A=infinity, C_π=35 pF and c_μ=4pF **(13) [ID] (May/June 2016)**



5. Explain about the high frequency response of common source and derive the expression for lower cut off frequency and upper cut off frequency **[D] (13) (April/May 2014, Nov/Dec 2014)**
6. Find the Mid band gain AM and upper 3 - dB frequency hi of a CS amplifier fed with a signal source having an internal resistance Rsig = 100 KΩ. The Amplifier has RG = 4.7 MΩ, RD = RL =15 KΩ, gm=1 mA/V, ro=150 KΩ ,cgs= 1pF and Co = 0.4pF. **(15) [ID] (April/May 2017)**
7. For the circuit shown in Figure 14, let V_{DD} = Vss =1.5 V, V_{tn} = 0.6 V, V_{tp} = -0.6 V, all channel lengths = 1µm, K_n = 200 µA/V^2, Kp =80 µA/V^2 and λ = 0. For I_{ref} =10 µA , find the widths of all transistors to obtain I_2 = 60 µA, I_3 = 20 µA and I_5 = 80 µA . It is further required that the voltage at the drain of Q2 be allowed to go down within 0.2 V of the negative supply and voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply. **(10) [ID] (April/May 2015)**



8. For the circuit shown find the cut off frequencies due to c_1 and c_2 with hfe = 100 and hie = k ohms.**(6) [D] (April/May 14)**



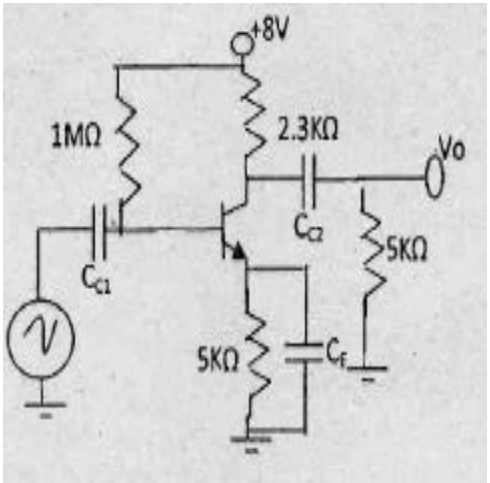
BJT frequency response

9. Derive the expression for cut off frequency of a BJT**. (13) [D] (Nov/Dec 2016)**

[SECOND HALF]

fα, fβ and unity gain bandwidth

10. Explain hybrid π CE short circuit current gain. Derive the expression for $f_\alpha, f_\beta, f_\gamma$. **(13) [D] (April/May 15)**
11. Derive the expression for $f_\alpha, f_\beta, f_\gamma$ **(7) [D] (April/May 2014)**
12. Define f_α and f_β and fτ. And also derive for f_α and f_β and fτ with two source terminal and one sink terminal currents as a function of reference current. **(13) [ID] (Nov/Dec 2017)**
13. Derive expressions for the short circuit current gain of common emitter amplifier at High Frequency. Define alpha cut-off frequency, beta cut-off frequency and transition frequency and derive their values in terms of the circuit parameters. **(13) [D] (April/May 2017)**
14. Derive for f_β and fα. **(6) [D] (Apr/May 2015)**
15. For the circuit shown in below Figure has following parameters: hfe =125 , Cπ= 24 pF, Cμ = 3 pF (1)Determine its mid-band gain, upper-cut off frequency. (2) Find the value of Cc_1 , C_{c2} and CE by assuming lower cut-off frequency of 100 Hz. **(10) [D] (Apr/May 2015)**



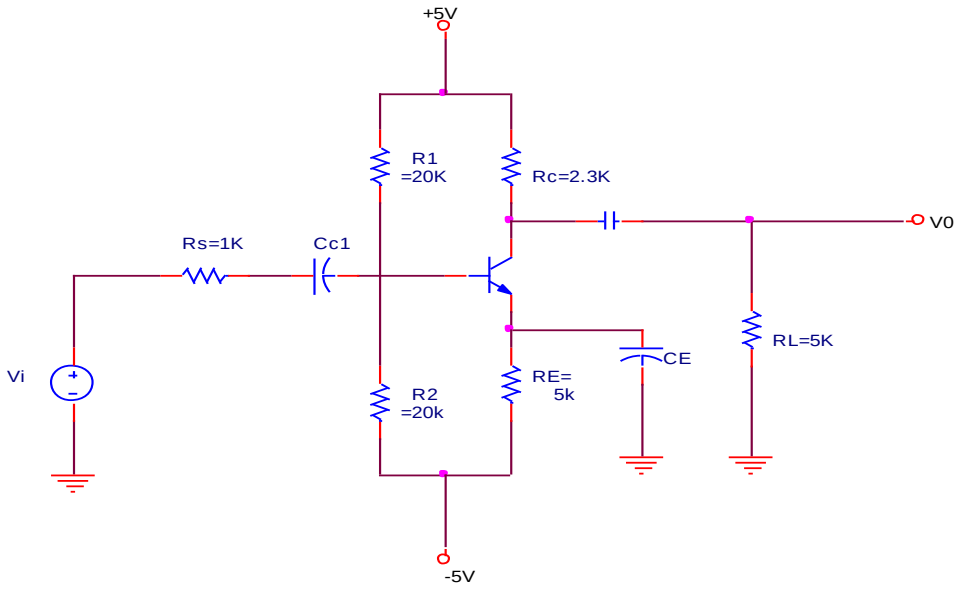
Miller effect

16. Explain in detail about the Miller theorem and Miller effect **(7) [D]**
17. What is multistage amplifier .Explain about the frequency response for multistage amplifier. Derive the expression for overall upper and lower cutoff frequency of the same.**(13) [D]**
18. The transistor in the figure has parameters β =125, $V_{BE(ON)}$=0.7 V, V_A=200 V, C_π=24 pF and c_μ=3pF. **(13) [ID] (May/June 2016)**

    (i) Calculate the miller capacitor

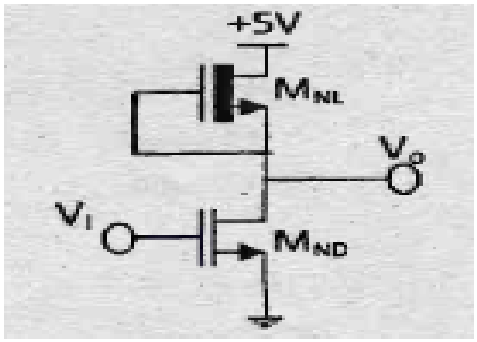
    (ii)Determine the upper 3 dB frequency

    (iii)Determine the small signal mid band voltage gain

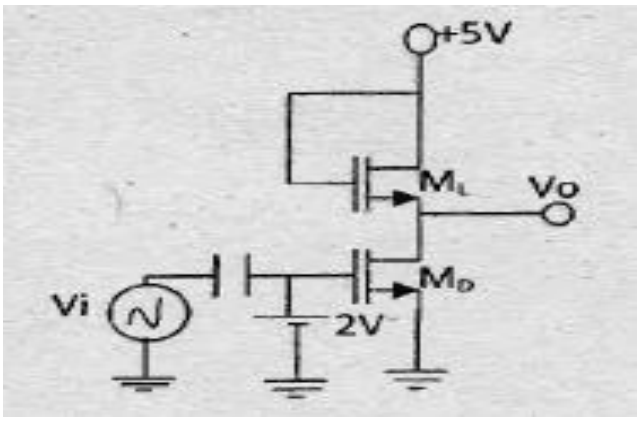


Frequency Response of **FET, High frequency analysis of CE and MOSFET CS amplifier**

19. Explain the high frequency analysis of JFET with necessary circuit diagram and derive its gain bandwidth product. **(13) [D] (April/May 2018)**
20. Construct the high frequency equivalent circuit of MOSFET from its geometry and derive the expression for short circuit current gain in the common source configuration**. (13) [D] (Nov/Dec 2016)**
21. Determine the voltage gain, input impedance, output impedance of CMOS source follower amplifier**. (13) [D] (April/May 2015)**
22. Consider the circuit of NMOS amplifier with depletion load (shown in below fig) The transistor parameters are V_{TND} = 0.8 V, VTNL = -1.2 V, β_{nd}= (μ_{nD}Cox(W/L)) = 500 μA/V^2, β_{nL} = (μ_{nD}Cox(W/L)) = 50 μA/V^2, I_{DQ} =100 μA , V_{DD} = 5 V and λ_{nD} = λ_{nL} = 0.01 V^{-1}. (1) Determine V_{GS} such that the Q-point is the mid of the saturation region. (2) Calculate Q-point drain current. (3) Determine the small signal voltage gain. **(8) [ID] (April/May 2015)**



23. For the NMOS inverter circuit with saturated load (shown in below), the transistor parameters are: (device data for M_D: V_{tnD} =1 V , $K_{np} = \mu_n Cox(W/L) = 100\ \mu A/V_2$, $\lambda_{nD} = 0$ and device data for M_L : V_{tnL} =1 V , $K_{nL} = \mu_n Cox(W/L) = 20\ \mu A/V^2$, $\lambda_{nL} = 0$ Draw its voltage-transfer characteristics curve, and mark down its transition points. **(6) [ID] (April/May 2015)**



UNIT-V

POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

PART A

1. How does a MOSFET work an amplifier? **[ID] (April/May 2018)**
2. Draw the symbols of PMOS and NMOS. **[D] (Nov/Dec 2017)**
3. Why active loads are not used with discrete Circuits?**[ID] (Nov/Dec 2016)**
4. Define CMRR? **[D] (Nov/Dec 2016)**
5. Mention the different types of active loads **[D] (Nov/Dec 2015)**
6. List out the advantages of CMOS differential amplifier over MOS differential amplifier. **[D] (A/M '15)**
7. Comparison between BJT and MOSFET.**[D]**
8. Comparison between capacitor input and LC filter **[D]**
9. State the advantages of π filter. **[D]**
10. State the Disadvantages of π filter. **[D]**
11. Sketch the block schematic of regulated power supply. **[D]**
12. Comparison of shunt and series regulators **[D]**
13. What is the need of SMPS? **[D]**
14. Derive the ripple factor of FWR.**[ID]**
15. What is a bleeder resistor? State its use.**[D]**

16. Define transformer utilization factor. State its value for half wave rectifier. **[ID]**
17. Define ripple factor **[D]**
18. Derive the ripple factor of HWR. **[ID]**
19. Define peak inverse voltage. **[D]**
20. Define line regulation and load regulation. **[D]**
21. Where is SMPS used? **[D]**
22. What are advantages of SMPS? **[D]**
23. State any two reasons unregulated power supply is not suitable for many applications. **[ID]**
24. How shunt regulator is differentiated from series regulator? **[ID]**
25. Write down the expression of ripple factor of L filter in FWR. **[D]**
26. Draw the full wave bridge rectifier circuit **[D]**
27. Compare the performance of half wave rectifier and full wave rectifier. **[D]**
28. Why is a simple capacitor filter not suitable for heavy loads? [I**D]**
29. Draw the diagram of CLC filter. **[D]**
30. Draw the transistorized series feedback type regulator. **[D]**

PART B

[FIRST HALF]

Half-Wave Rectifier Power Supply

1. Derive the expression for the rectification efficiency, ripple factor, transformer utilization factor, form factor and peak factor of half wave rectifier. **(8) [D]**
2. Draw and explain the working of half wave rectifier. **(8) [D]**

Full-Wave Rectifier Power Supply

3. Draw and explain the working of Full wave rectifier. **(8) [D]**
4. Derive the expression for ripple factor of LC filter with full wave rectifier. **(8) [ID]**
5. Explain the working of FWR with CLC filter and derive for its ripple filter? **[ID] [13]**
6. Derive the expression for the ripple factor of π filter with full wave rectifier. **[ID] [4]**

Voltage regulators - series, shunt and switching Voltage Regulators

7. Draw a neat diagram of a series regulator and explain its working? **(8) [D]**
8. Explain the circuit of voltage regulator and also discuss the short circuit protection mechanism. **(15) [ID]**
9. With a neat diagram explain the operation of transistorized series type voltage regulator (**13) [D]**
10. Draw the circuit and explain the operation of voltage inverter type switching regulator. **[D] (13)**

[SECOND HALF]

Switched mode power supply

11. How output voltage can be regulated with respect to line and load variations using SMPS? **(10) [D]**
12. Draw the block diagram of a switched mode power supply and explain the operation. State its advantages. **(15) [D]**

BJT and MOSFET

13. With the necessary diagram explain about CMOS differential amplifier and derive the CMRR. **[D] (16) (April/May 2016)**
14. Draw and explain the MOSFET Cascode current source circuit and also discuss its advantages. **(13) [D] (April/May 2018)**
15. Describe the operation of a PMOS amplifier with an enhancement load and a depletion load with necessary diagrams. **(13) [D] (April/May 2018)**
16. Describe the working principle of Basic MOSFET current source circuit with neat circuit **(13) [D]**
17. Describe the working principle of Basic MOSFET current mirror circuit with neat circuit **(13) [D]**
18. With the analysis, explain about MOSFET current steering circuit. **(13) [D] (Nov/Dec 2017) (Apr/May'17)**
19. Draw and explain the operation of a simple MOSFET amplifier with active load and derive its voltage gain using small signal equivalent circuit. **(13) [D] (Nov/Dec 2016)**

DC regulated Power supplies

20. Discuss about the electronically regulated d.c. power supplies **[8] [D]**

**********All The Best**********